ADV DIGITAL SYSTEM DESIGN
MID TERM EXAM

Time: 2:00 Hrs
Marks: 60
Instructor: Dr Shoab A. Khan

Question 1: Verilog Coding

(a) Design **architecture** and implement it in RTL Verilog to realize the following difference equation;

$$y[n]=x[n] - x[n-1] + x[n-2] + y[n-3]+0.5y[n-1]+0.25y[n-2];$$

(b) Write RTL Verilog Code (stimulus is not required) to implement Multiply Accumulator (MAC) architecture. The design implements the following:

$$Acc = A \times B + C \times D + Acc$$

The signals A, B, C, D and Acc are 8, 8, 8,8 and 32-bit wide unsigned numbers respectively.

7, 8

Question 2: Fixed-point Conversion

(a) Using 16-bit fixed-point arithmetic draw a second order cascaded structure for the filter given by the following transfer function in double precision floating point format:

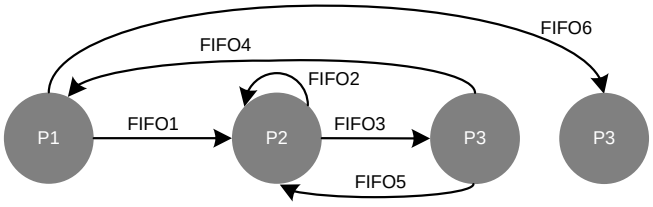
$$H(z) = \frac{2.3457\,(1 - 0.9231z^{-1} + 5.231z^{-2})(1 + 1.223z^{-1} + 2.125z^{-2})}{(1 - 0.1546z^{-1} + 0.9231z^{-2})(1 - 0.221z^{-1} + 0.9114z^{-2})}$$

(b) Convert the coefficients in appropriate 10-bit fixed-point format and write RTL Verilog code to implement one of the cascaded second order section.

(8,7)

Question 3: DFGs

Map the following DFG to KPN architecture.



(15)

Question 4: ADDERS

Draw an 8-bit Conditional Sum Adder architecture to compute the expression

if(A-B)

Show the working of Conditional Sum Adder architecture on the following numbers:

A = 1001_1101

B = 1101_1011

(15)